AMENDMENT TO THE SPECIFICATION

Please replace the paragraph at page 3, line 20 – page 4, line 14 with the following amended paragraph:

The preferred embodiments presented herein provide a technique to delete data in a write-once memory device while avoiding the performance degradation and memory design modifications associated with the approaches discussed above. Some of these preferred embodiments take advantage of error protection schemes to alter bits stored in the write-once memory device. As used herein, the term "error protection scheme" refers to any technique that uses a plurality of syndrome bits and a plurality of data bits to detect and/or correct certain types of errors in the word containing the plurality of data and syndrome bits. Suitable error protection schemes include, but are not limited to, error correcting code (ECC), Reed-Solomon, BCH, Golay, and Viterbi. The preferred embodiments will be described with reference to an ECC scheme using a Hamming (k, n) code. With the Hamming (k, n) code, (k-n) syndrome bits are used to identify and correct a single-bit error in a word of k bits. The presence of two or more errors in the k-bit word cannot be corrected. While it is preferred that a Hamming (72, 64) code scheme be implemented, for simplicity, a Hamming (7, 4) code scheme will be used to illustrate these preferred embodiments with the bit layout depicted in Figure 1. The seven-bit word in Figure 1 contains four data bits (bits 4-7) and three syndrome bits (bits 1-3). The first syndrome bit (bit 1) is the parity of data bits 4, 5, and 7; the second syndrome bit (bit 2) is the parity of data bits 4, 6, and 7; and the third syndrome bit (bit 3) is the parity of data bits 5, 6, and 7. While the syndrome bits are located adjacent the data bits in Figure 1, the syndrome bits can be dispersed within the word or located in a different part of the memory device. It is preferred that data and

syndrome bits be distributed in the write-once memory device using the technique described in "Memory Device and Method for Storing Bits in Non-Adjacent Storage Locations in a Memory Array," U.S. Patent Application Serial No. 10/024,647 —— (Attorney Docket No. 10519/60, filed on the same day as the present application), which is hereby incorporated by reference.